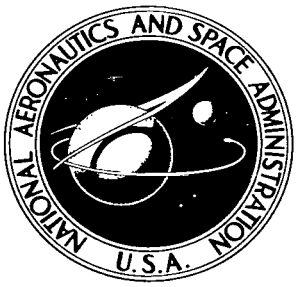
NASA TECHNICAL NOTE



NASA TN D-4224
c.1

NASA TN D-4224

PRESENT AND FUTURE STATE OF THE ART IN GUIDANCE COMPUTER MEMORIES

by Robert C. Ricci

Electronics Research Center
Cambridge, Mass.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • NOVEMBER 1967

NASA TN D-4224

PRESENT AND FUTURE STATE OF THE ART IN GUIDANCE COMPUTER MEMORIES

By Robert C. Ricci

Electronics Research Center
Cambridge, Mass.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 – CFSTI price $3.00

PRESENT AND FUTURE STATE OF THE ART IN GUIDANCE COMPUTER MEMORIES

by Robert C. Ricci
Electronics Research Center

ABSTRACT

A survey of the present and anticipated state of the art for 1970-1972 in guidance computer main memories is presented. The selection of memory components for use in advanced guidance computer applications motivates the work reported. Non-destructive read-out (NDRO) vs. destructive read-out (DRO) type memory techniques and technologies are discussed, with particular reference to six types of advanced solid-state memory devices: magnetic cores, plated wire, planar-magnetic thin films, etched-permalloy toroids, monolithic ferrites, and integrated-circuit memories. Present characteristics of these devices are compared, and a summary of anticipated characteristics of memory devices for 1970-1972 is detailed. Memory technologies available for implementation of a system-concept breadboard in 1967, as well as those most likely available for a prototype advanced guidance computer for flight in 1970-1972, are likewise identified.

INTRODUCTION

Storage devices and memory technology continue to play an important role in the development and progress of digital computers. Increasing memory capacity and speed are enhancing the capability and flexibility of modern computers. To implement the concepts of modularity and multiprocessing in advanced guidance computer applications, memory technology and techniques will occupy an even more dominant role in future space computers. The development of faster, larger in capacity but smaller in size, cheaper, and more versatile memories than those now available is anticipated.

The goals in the selection of a memory technology for advanced guidance computers are high reliability and low power. A component memory survey has recently been completed. Its objectives were (a) to determine the state of current memory technology, (b) to evaluate the probable state of the art relative to a high-reliability space application, and (c) to find hardware representative of the technology of item (b) available in 1967 for use in a system-concept breadboard.

In future advanced guidance systems, it appears that memory capacities of 0.2 to 1×10^6 bits and read-write cycle times of 1 to 2 μsec or less are needed. Also, add speeds of 2 to 4 μsec and multiply times of 10 to 20 μsec may be required. These characteristics guide the work reported in this document.

The following technologies are considered for use in advanced guidance computers:

1. Magnetic Cores
2. Plated Wire
3. Planar-Magnetic Thin Films
4. Etched-Permalloy Toroids
5. Monolithic Ferrites
6. Integrated-Circuit Memories.

Visits to a number of industrial laboratories assisted evaluating the present state of these technologies, as well as extrapolating the expected progress of the more promising technologies for 1970-1972.

Hobbs (ref. 1) previously described the present and future state of the art in commercial computer memories, but this document emphasizes aerospace guidance memories and techniques. NDRO and DRO memory elements are compared and discussed in detail.

It is not possible to review in detail all memory techniques presently available. In a report such as this, some pertinent accomplishments may be inadvertently omitted; others, which are included, may not be given the emphasis they deserve.

GENERAL CONSIDERATIONS

The primary consideration encompasses some of the characteristics desirable in a main memory for a guidance computer. A spaceborne or aerospace memory must be able to store information without error for extended periods of time and under adverse environmental conditions. For an advanced guidance computer, accordingly, reliability is the most important factor. Other important areas for comparison, which vary in importance depending on the intended mission of the computer, are volatility, power consumption, speed, cost, volume, weight, temperature sensitivity, mechanical strength, and magnetic tolerance. These factors are interrelated, and must be traded off against one another.

DRO vs NDRO

The most common space-qualified destructive read-out (DRO) memory in existence today is the coincident-current ferrite core. Planar film DRO memories exist, but are not in wide use in aerospace applications. After completion of a read cycle, the DRO elements are permanently disturbed so that the memory electronics must be re-energized to remagnetize the elements, thereby restoring the memory word.

Two general types of non-destructive read-out (NDRO) memories are available. In the first type, called "read only" (ROM), the information is mechanically written by threading wires, punching holes, or cutting wires by some relatively permanent means. In the second type, electronically alterable, the information is written into the memory in a manner similar to the DRO memory. Reading is also similarly performed as in the DRO case, but the magnetic disturbance produced by the read current is self-reversible, that is, the element returns to its initial state. This removes the requirement of a restore cycle.

Since, in most missions, the computer program is stored in memory, where the loss of all or any portion of this program makes the computer inoperative, protection of the stored program under adverse conditions, such as temporary power failure or excessive electrical transients, is necessary.

Because the DRO memory must maintain on-line electronics capable of delivering write-current pulses, the possibility of temporary electronic malfunction may cause the alternation of information.

The NDRO memory, whose program may be entered by means of auxiliary support equipment, however, or whose writing electronics may be disabled during a mission, is only capable of producing false read-current pulses caused by electronic malfunctions. An additional benefit of an NDRO memory is reduction in power consumption because the elements are self-restored and do not require electronic restoration. If the number of read commands is much greater than the number of write commands, as is usually the case, this saving in power is evident. A third advantage of NDRO is speed. In DRO memories, a major portion of the R-W cycle time is spent performing the write operation. The major limitation in core memory systems is the inhibit recovery time. The sense amplifier must recover from the large write transient.

To make an overall evaluation of these two types of memory systems, the proven reliability of DRO core memories vs. the advantages of NDRO devices must be traded off. Some of these advantages are proved; others are not. Most of the NDRO memory elements are still in the laboratory developmental stage.

MEMORY TECHNOLOGIES

Magnetic Cores

Magnetic cores are presently the dominant technology in spaceborne memory systems. Three major types of core memories now exist: linear select (2D), coincident current (3D), and a compromise (ref. 2) between coincident-current and linear-select organizations (2-1/2D).

Linear-select memories are the most expensive form of memory organization, because of the word driver circuitry, but fastest, because more than the minimum switching current can be applied to the ferrite core to increase its switching time. Coincident-current (CC) memories are cheapest, because less selection and addressing electronics are required, but these have the disadvantage of a long-inhibit recovery mode that limits the present speed of CC memory systems to a 1-μsec R-W cycle time, and probably a limitation of 700 nsec by 1970-1972.

The 2-1/2D organization permits faster operation than a coincident-current memory and lower cost than a linear-select memory, and is the trend in commercial core-memory systems. Most of the major core manufacturers have plans to announce 2-1/2D core-memory systems using 20/12 mil cores (O. D. =20 mils, I. D. =12 mils) by the end of the year, with cycle time ranging from 500 to 650 nsec for memory modules of 8 to 16K words having 24 to 36 bits per word.

Another trend is the use of wide-temperature lithium ferrite cores, rather than the manganese magnesium cores now presently used. This is analogous to the relatively recent trend from germanium to silicon in the semiconductor area. The basic reason for this change is the increase in power dissipation in the ferrite core because of the faster memory-cycle times.

The emphasis in commercial core systems is in lower costs and faster cycle times, and all developments point in these directions. Although the above two factors are important to advance guidance computer programs, the primary goals of NASA are reliability and low power.

A new packaging scheme just recently developed eliminates the center supports in core arrays so that it is now possible to stack 12 bits per inch, rather than the usual 8 bits per inch. The packaging densities available with cores are presently 1600 bits/in.^{2} because of the use of smaller cores (20/12 mils). The half-select currents needed for switching are 400 mA for a 1-μsec memory cycle time with 30/18 mil cores. The above packing densities and current requirements compare very favorably with other technologies.

For space applications, it appears desirable to have a core that requires switching currents of less than 200 mA, so that integrated circuit drivers can be used, and yet furnish a switching speed of 300 nsec, to make a 1-μsec cycle time feasible. Research programs are in progress to develop low-current, wide-temperature cores, but with a goal of 3- to 4-μsec cycle time.

There are many predictions that other technologies are to replace magnetic cores, but magnetic-core technology is so widespread and established that it is difficult for other technologies to replace it. The core suffers, however, from the limitation of only DRO operation, unless more sophisticated geometries are used such as the multi-aperture devices (MAD) or Biax.

The multi-aperture devices use the technique of two or more holes whose axes are parallel. By means of an appropriate pattern of conductor wires, a flux pattern can be set up to give NDRO operation, although a prime current cycle is required after every interrogate pulse. A memory of this type is very expensive, and requires relatively intricate wiring and has severe temperature limitations. Two devices (ref. 3) using this technique are the transfluxor and the Shmoo element. The currents required for these devices are high, 900 mA for clear and 550 mA for set, with a minimum read-modify-write time of 4 to 5 μsec.

The Biax (ref. 4) is a block of pressed, square-loop ferrite material with orthogonal, non-intersecting holes. Readout is derived from flux interference in the common volume of material between the holes. Binary state of the element is determined by polarity of remanent flux around the storage hole. Various operating modes are possible. A two-wire scheme operating in a "ratchet-write" mode is usually used. The Biax is capable of high-speed (20 MHz) read-out operation, but for a read-modify-write mode is limited to about 5 μsec. Required write current is 360 mA. The Biax is temperature-sensitive because its B-H loop is non-square and, therefore, extensive current compensation is needed. Its curie temperature is 200° C. The usual application of Biax elements is in bootstrap operations, where the information is loaded

on the ground with test support equipment and then operated in a read-only mode in flight.

The status of both the Biax and the Shmoo was reviewed in the course of the survey. No perceptible effort is presently being expended to improve either of these techniques, however, so that no significant improvements in materials or geometries can be expected by 1970-1972.

Plated Wire

This is a type of magnetic film memory fabricated by plating a magnetic film on a wire substrate. A cylindrical film has advantages over planar films in having a closed flux path in the digit direction, and thus lower digit currents are required and a larger sense signal is obtained.

A 10,000-angstrom permalloy film is plated on a 5-mil beryllium copper wire. This wire serves as the plating substrate, as well as the digit sense wire. The plating process applies a bias current down the wire to give a magnetic easy-axis circumferential to the wire. The magnetic material is electroplated on a continuously moving wire in a room environment.

Basically, two types of plated wire memories are available, the strip-line technique (ref. 5) and the woven-wire approach (ref. 6).

In the strip-line technique, the word drivers consist of flat metal strips placed over the digit wires. These word-drive straps are either returned under the digit wires or terminated in a ground plane beneath the digit wires. The digit lines are typically on 30-mil centers and the word straps on 50-mil centers, giving a packing density of 700 bits/in.^{2}.

The second type makes use of a weaving process to fabricate the memory planes. The plated wire is woven into a matrix at right angles to insulated word-drive lines by means of a large automatic loom. The rest of the process is very similar to the strip-line technique. The woven wire provides a tighter magnetic coupling than in the strip-line approach, and also enables easier implementation of multiple turns in order to reduce the drive currents. It has more capacitative coupling, however, than the strip-line technique.

The plated-wire device is capable of both NDRO and DRO operation. For NDRO operation, the required drive currents for the strip line version are $I_W = I_r = 360$ mA and $I_d = 40$ mA, with a worst-case sense voltage of 2.5 to 5 mV. Tolerances on all currents are ± 10% for a 0 to 50° C temperature range, without compensation of drive currents. With compensation, NDRO operation is feasible from -10 to +85° C. Equal read and write currents may be used, giving the plated-wire memories multiword organization capability and all the advantages of NDRO operation, as previously described. Although the plated-wire organization is basically linear select because of multiword organizations, it is possible to minimize the number of digit drivers and sense amplifiers. With equal read and write currents, it is also possible to simplify the word driver electronics.

For the woven-wire planes, the required currents are read 265 mA, write 500 mA, and digit 65 mA. The output-sense voltage is 2 mV for a 50-nsec rise-time, read-current pulse. Also, memory planes which require equal read and write currents are now available.

One large computer organization has announced use of NDRO plated-wire memories in a new series of computers with a capacity of 16,000 bytes (9 bits/byte) and a read-write cycle of 600 nsec. Also, a fully qualified 1024-word, 24-bit-per-word plated-wire memory stack for a military program with a 2-μsec R-W cycle is presently being developed. This memory has NDRO capability and uses equal read and write currents. Other programs with government agencies to develop woven-wire memory stacks ranging in size from 512 words to 4096 words and with speed requirements of 2 μsec or slower are in development. In addition, most of the companies visited have at least small plated-wire memory programs, even though their major effort may be in a different technology.

Although the plated-wire technology has many potential advantages, it is not without problems. The major problem is an aging effect, where it is found that NDRO properties of the plated wire deteriorate over a period of time. It is thought that the problem is due to stress of the plated wire after plating or to Cu migration from the beryllium Cu substrate wire to the permalloy plated film, which changes the film's magnetic properties. An additional problem is that of adjacent word disturbs, which is basically a creep, skew, and dispersion problem. This limits the packing density presently to about 700 bits/in.^{2} and current tolerances in NDRO mode.

Extrapolations to 1970-1972 indicate an increase in packing density and reduction of drive currents compatible with the current-driving capabilities of integrated circuits by reducing the size of the beryllium copper wire from 5 mils to ~ 1 mil in diameter. Plated wires also are being designed for use in scratch-pad and fixed-memory applications, and thus have the potential advantage of use in all memory applications of a future guidance computer.

Planar-Magnetic Thin Films

At present, planar films are used primarily in small high-speed control and scratch-pad memories. The past 10 years show slow progress in this film technology, which suffers from the handicaps of a number of difficult processing steps, as well as an open-flux structure resulting in small sense signals and a tendency to demagnetize along the outer edges of the bit spot. These limit the thickness of the film and, thus, the output-sense signal. Other problems include dispersion, skew, magnetostriction, and high-drive currents.

A thin magnetic film NDRO element, such as the Bicore (ref. 7) or Quadralloy* element, exists, however, and shows promise for use in NDRO main memory applications. The Bicore element is flight-qualified and is used in aerospace computer memory systems. The Quadralloy element is presently being incorporated in the Phoenix guidance computer system. In both of these applications, however, information is loaded into memory by test support equipment, and then operated in a read-only

*Trade name

mode in flight. In a read-modify-write mode, present achievable cycle times are 7.5 μsec, and high drive currents 1.5 A for write, 800 mA for read, and 100 mA for digit are needed. Densities are similar to those obtainable with planar thin films, 600 bits/in.^{2}.

These elements consist of "soft" and "hard" magnetic layers. The soft layer can be subjected to relatively modest magnetic fields, whereas the hard layer must be influenced by a much larger field to cause a change in its magnetization. During writing operation, a large field is applied to switch the hard film to the desired state. During read, a smaller field is applied to the soft film to produce a signal output. The relatively uninfluenced hard film provides the restoring field to bring the soft film back to its original state, and this gives NDRO operation.

Recent developments by Pohm (ref. 8) at Iowa State University show promise for this device. Pohm has developed an element with a fine geometry with multiturn word lines requiring 30 mA for read and 80 mA for write, with an increase in packing density of 10 over conventional thin-film arrays to ~ 800 bits/in.^{2}. Since integrated circuits can easily supply this current by 1970-1972, it may be possible to have an all-integrated Bicore memory system. This small Bicore element has been shown to operate in read-modify-write mode of less than 500 nsec in modest size arrays, 128 bits.

The disadvantages of this approach are: (a) non-competitive cost with core memories because of low yields and inability to make large arrays with uniform properties, (b) small output signals – 1 mV, and (c) long-term "disturb" sensitivity.

Another development in the magnetic film area is the multi-layer film structure, in which two layers of magnetic film of similar composition are vacuum-deposited, first one and then a second, to enclose an inner conductor, the digit-sense wire. In essence, the element has a closed flux path in the digit direction, but not in the word direction, and thus low-digit drive currents are possible, 15 to 20 mA. Although most of the effort at the present time is directed towards DRO multilayer film memories, an optimum space-memory element may be one that uses two different magnetic film layers (different magnetic compositions), as in the Bicore element, but fabricated by use of the multilayer film technique. Such a structure possesses inherent NDRO properties based on a steering field that the hard film provides. This steering field restores the soft film back to its original state; and, therefore, the element has a higher magnetic tolerance and less sensitivity to noise than present-day devices.

Etched-Permalloy Toroids

In this technique (ref. 9), a permalloy sheet is etched in a pattern to give a matrix of toroidal-permalloy storage elements. A number of plating and etching processing steps is required to fabricate the conductors that serve as the drive and sense lines for the memory plane.

An 8K-word, 30 bits/word, DRO, aerospace memory using this technique is being developed. It has a 2-μsec R-W cycle, a volume of 64 in.^{3}, power dissipation of less than 10 W, and is operated in a linear-select mode. Low currents capable of being implemented by present-day integrated circuits are required for operation, I_r = 150 mA, I_w = 120 mA, and I_d = 50 mA.

Presently a 10^8-bit NDRO mass memory is also being developed, under contract to the Air Force, using this memory technique. It is a three-wire, coincident-current memory system using 23/17 mil toroidal cores. It has a R-W cycle time of 35 μsec and an access time of 15 μsec and operates in an NDRO mode by using an rf-sensing scheme.

In summary, the permalloy-toroid approach requires a very large number of processing steps and interconnections. The elements consist of multilayer structures that have different chemical compositions, and the technology requires the conversion of KTPR from a photographic material to an insulating material. The permalloy material is very non-square, and has a slow switching-time coefficient that limits its speed capabilities to $\sim$ 2 μsec. Its big asset is low drive requirements. The technique does not appear suitable for NDRO fast main memory systems. When low power, size, and weight are important, however, it shows considerable promise.

Monolithic (Laminated) Ferrites

The monolithic ferrite technique (ref. 10) is a batch-fabricated approach. The basic operations involved in fabricating a monolithic memory are doctor-blading, laminating and sintering, and conductor screening. The array planes are fabricated in array sizes of two types, 64 x 64 crossovers or 256 x 100 crossovers. Planes are fabricated by laminating three sheets of doctor-bladed ferrite. After sintering, the ferrite shrinks to an overall thickness of 5 mils, with a conductor spacing of 10 or 15 mils to give packing densities of 10,000 bits/in.^{2} or 4000 bits/in.^{2}

Two types of ferrite material are available for use in this technique: (a) a high-current drive, fast-switching material (0.1×10^{-6} oersted-sec) and (b) a low-drive slow-switching material (0.5×10^{-6} oersted-sec). Both materials have relatively low curie temperatures (262° C), making temperature compensation of the drive currents beyond a range of 0 to 50° C necessary. However, laboratory tests indicate a possible extension of this range to -25 to +75° C. The currents for the high-drive material are I_r = 440 mA, I_w = 110 mA, and I_d = 35 mA, and for the low-drive material I_r = 100 mA, I_w = 70 mA, and I_d = 15 mA. Sense voltages are 5 to 10 mV for the high drive and 3 mV for the low drive.

Present operation of monolithic ferrites is confined to a DRO, linear-select mode. The memory device possesses no inherent NDRO properties, although various schemes are used to obtain NDRO operation.

Fabrication of the large memory arrays, 256 x 100, with acceptable yield and uniformity is necessary for the technique to compete favorably with other advanced memory techniques.

At the present time the fabrication of the large arrays is in the laboratory stage. By use of these 256 x 100 memory arrays, it is possible to reduce significantly the number of required interconnections in memory modules. From a reliability point of view, the present method of connection from the drive circuitry electronics to the embedded conductor in the ferrite wafers needs investigation.

A research program is in progress in industry, however, to develop MOS word-drive electronics for the low-drive ferrite material, so that a fully integrated memory system may be feasible. Nevertheless, the monolithic ferrite technique does not appear promising for main memories for guidance application, where a NDRO element is desired and 1-μsec or less R-W cycle times are needed. It may have application in large capacity memory applications, where size is of prime importance, because of its excellent packing density, 10,000 bits/in.^{2}, and low-drive current requirements.

Integrated Circuits

For scratch-pad or high-speed control applications, there is little doubt integrated circuits are to become the dominant technology in 1970-1972, replacing planar thin films currently being used. For a capacity of 10^4 bits, a R-W cycle time of 50 nsec is feasible for bipolar integrated circuit arrays and a R-W cycle time of 150 nsec for MOS arrays.

Although integrated circuits have been proposed for main memory applications, they are not being considered seriously because of their volatility and active element characteristic. The power required per stage is a serious problem when memories of large capacity are considered.

Arrays of 16 bits (bipolar) are available from several vendors and arrays of 64 bits are expected by the end of 1967. Power dissipation per bit is relatively high, 10 mW. An experimental scratch-pad memory (256 words, 72 bits with a 150-nsec write cycle time) from small arrays of four words of nine bits each on single 60-x-80-mil chips is available.

Other programs are being pursued to develop 1000-gate arrays. One program is concentrating on MOS-FET* arrays, another on bipolar, and a third on a combination of MOS and bipolar arrays, where the decoding circuitry is bipolar and the memory elements are MOS.

Summary of Characteristics

A summary of characteristics for present state of the art main memory storage devices is detailed in Table I, and a summary of an estimate of characteristics for main memory devices for 1970-1972 is illustrated in Table II.

READ-ONLY MEMORIES (ROM)

Although the main emphasis in the memory survey centers on main internal memories, a few words about the present technology of read-only memories appear in order. A read-only memory is one in which there is no electrical means of altering information. Memories using linear electrical coupling, R, L, and C arrays, non-linear coupling, diode, transistor, non-linear magnetic elements, and optical elements have been developed. ROM's are used because they offer speed, size, and cost advantages over electrically alterable memories.

---

*Metal-Oxide-Semiconductor-Field-Effect-Transistor

TABLE I. – PRESENT STATE OF THE ART FOR MAIN MEMORY STORAGE DEVICES

	Magnetic Cores	Plated Wire	Planar Film	Bicore	Monolithic (Laminated) Ferrites (High Drive)	Monolithic (Laminated) Ferrites (NDRO)	Etched Permalloy Toroid	Microbiax	Transfluxor Shmoo	Bipolar Intergrated Circuits
Read Speed, μsec	0.3	0.2	0.15	2.5	0.2	0.15	0.7	0.5	1 - 2	0.15
R-W Cycle, μsec	0.7	0.6 to 2.0	0.5	7.5	0.5 - 2	0.5 - 2	2.0	4.5	4 - 5	0.30
Typical Capacity (Bits x 10^6)	2.0	0.15	0.8	0.3	0.25	0.1	0.24	0.2	0.15	0.02
Mode of Organization	2-1/2D	LS*	LS	LS	LS	LS	LS	LS	CC**	LS
Batch Fabrication	No	Semi	Yes	Yes	Yes	Yes	Yes	No	No	Yes
Volatility	No	No	No	No	No	No	No	No	No	Yes
NDRO	No	Yes/No	No/Yes	Yes	No	Yes	No	Yes	Yes	Yes
Packing Density (bits/in.^{2})	1600	500 - 800	600 - 800	600 - 800	4000	4000	1600	900	400	7200
Read Current, mA	400	250 - 900	600	500 - 800	400	90	150	300	±300	25
Write Current, mA	400	250 - 900	600	2000 - 3000	100	-350 +120	120	±360	+900 -350	55
Bit Current, mA	400	40 - 65	±100	100	35	30	50 - 60	±100	±150	10
Sense Voltage, mV	18 - 20	±2.5 - 5	±0.5 - 1.5	±0.5	4 - 10	2.5	1 - 2	12	25	30 - 2000
T_r (Typical Rise-time of Read Current), nsec	50	45	10 - 35	45	45	10	150	40	100	-
Curie Temp., °C	600°	550° - 600°	600°	600°	200° - 300°	200° - 300°	550°	200°	200° - 300°	-

*(LS) Linear Select
**(CC) Coincident Current

TABLE II. – ESTIMATE OF CHARACTERISTICS FOR MAIN MEMORY DEVICES FOR 1970-1972

	Magnetic Cores	Plated Wire	Planar Film	Bicore Multilayer	Monolithic (Laminated) Ferrites (High Drive)	Monolithic (Laminated) Ferrites (Low Drive)	Etched Permalloy Toroid	Microbiax	Transfluxor Shmoo	Bipolar Integrated Circuits	MOS Arrays
Read Speed	0.1 - 0.3	0.1	.07	0.1	0.2	1.0	0.7	0.5	1 - 2	0.07	0.2
R-W Cycle, μsec	0.3 - 1	0.3	0.2	0.3	0.5	2.0	1.5	4.5	4 - 5	0.2	0.6
Typical Capacity (bits x 10^6)	1 - 10	6.0	2.0	1.0	3.0	3 - 10	6.0	0.2	0.15	0.5	0.8
Mode of Organization	2-1/2 D	LS*	LS	LS	LS	LS	LS	LS	CC**	LS	LS
Batch Fabrication	No	Semi	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes
Volatility	No	No	No	No	No	No	No	No	No	Yes	Yes
NDRO	No	Yes/No	No/Yes	Yes	No	No	No	Yes	Yes	Yes	Yes
Packing Density (bits/in.^{2})	4500	1450	3200	3200	10000	10000	1600	900	400	7200	15,000
Read Current, mA	400	200	150 - 200	60 - 75	400	100	150	300	±300	-	-
Write Current, mA	400	200	150 - 200	150 - 175	100	60	120	±360	+900 -350	-	-
Bit Current, mA	400	30	±25	25	35	±16	50 - 60	±100	±150	-	-
Sense Voltage, mV	20	2.5	±0.5 - 1.5	±2	4 - 10	±3	1 - 2	12	25	-	-
T_r (Typical Rise Time of Read Current), nsec	25	30	10 - 35	10	45	300	125	40	100	-	-
Curie Temp., °C	500° - 600°	600°	600°	600°	200° - 300°	262°	550°	200°	200° - 300°	-	-

*(LS) Linear Select
**(CC) Coincident Current

The most common ROM is the transformer type, one form of which is called the "core rope" (ref. 12) because of its physical resemblance to lengths of rope. The core rope consists of transformer cores threaded by a large number of word lines. The word lines either thread or bypass each transformer so that a "1" is represented by an output pulse and a "0" by the absence of a pulse when energized by a read pulse. Address decoding is designed into the wiring structure and, thus, high-bit densities (1500 bits/in.^{3}), including all electronics, can be achieved. Present efforts are directed at a variant of the transformer memory called a "braid" (ref. 13), which uses weaving with a loom as a means of manufacture to reduce the cost of fabrication.

A second type of ROM, holding considerable promise for use in 1970-1972, is the LSI diode or transistor matrix. A silicon-on-sapphire (SOS) technology (ref. 14), giving densities of 10,000 to 50,000 bits/in.^{2}, is available. This technique combines the active device properties and stability of bulk silicon with individual device isolation by thin-film evaporation on insulating substrates. The technology involves the deposition of a 1-micron thick layer of n-type single-crystal silicon on the surface of single-crystal alpha-aluminum oxide (sapphire). The present problem in this technology is the presence of a large number of dislocations in the deposited silicon layer resulting in leaky diode characteristics.

MIT is presently incorporating a silicon-on-sapphire read-only memory made up of 96-x-70 diode arrays for use in an alpha-numeric character generator.

SUMMARY AND CONCLUSIONS FOR 1970-1972

It is difficult to forecast the state of memory technology for 1970-1972 because of the rapid advances in this field. Nevertheless, it is possible to suggest the most promising possibilities on the basis of the direction of present and anticipated technological developments. Previous work (ref. 15) shows estimated computer memory capacity and speed requirements for advanced guidance computers to be 10^6 bits at most, and a 1- to 2-μsec or less read-write cycle time. These characteristics guide the conclusions presented in this report.

For hardware implementation of a prototype advanced guidance computer, either NDRO or DRO memory techniques may be used. NDRO techniques are less sensitive to electronic malfunctions or excessive electrical transients than DRO organizations, and require less power. Speed is also an advantage of NDRO, since a major portion of the R-W cycle time is spent in the write operation. However, NDRO memories tend to be less tolerant of environmental conditions, such as temperature and drive currents. Many factors that vary in importance, depending on the intended mission of the computer, such as reliability, volatility, power consumption, speed, cost, volume, weight, temperature sensitivity, mechanical strength, and magnetic tolerance, are interrelated and must be traded off against one another.

Among the more promising technologies for NDRO applications are the plated wire, elements of the Bicore variety, and the Biax. The plated wire technology offers many advantages; for instance, less sensitivity to transients, reduction in power, and increased speed. Extrapolations from the present time to 1972 indicate a reduction in

drive currents, making fully integrated systems feasible and increasing packing density. Also, by that time, plated-wire memory systems with R-W cycle times of 0.3 μsec may be available. There are, however, two problem areas – the aging effect and adjacent-word disturb. As noted previously, a deterioration occurs in the NDRO properties of the plated-wire film. Diagnosis and the solution to this aging problem are necessary. The second problem is that of adjacent-word disturbs, which is basically a creep, skew, and dispersion problem. This limits the packing density presently to about 700 bits/in.^{2} and the drive-current tolerances in the NDRO mode.

Elements of the Bicore variety, a laminar-magnetic element consisting of two magnetic layers, soft and hard, with NDRO properties, are flight-qualified from use in aerospace computers. The recent developments made by Pohm (ref. 8) of Iowa State make this approach promising. Here "fine" geometry Bicore-like elements that require low drive currents, I_r = 30 mA and I_w = 100 mA, are fabricated, and read-modify-write cycle times of 1 μsec are achieved. Also, by 1970-1972, Bicore-like elements and multilayer structure, fabricated by other techniques, may be in production.

Past space-memory programs have proven the Biax technique, although discrete, highly reliable. It has sense voltages of about 10 times those obtainable with the plated wire or Bicore technologies, and its packing density (900 bits/in.^{2}) compares rather favorably with the densities achievable from other techniques.

As for DRO applications, the most likely memory technologies for a prototype are the magnetic-core, the plated-wire, and the multilayer magnetic film elements. Extrapolation of current core technology indicates that 3D coincident-current core memories for memory capacities $\leq 10^6$ bits and for R-W cycle times $\geq$ 700 nsec will have been developed by 1970-1972. Anticipated development in 2-1/2D core organizations also include a potential speed capability of 300 nsec for 10^6 bit memories. The industry trend to reduce the size of the ferrite core to 16/10 or 12/7 mils may enable this increase in speed and capacity.

As previously noted, the plated-wire device is capable of both NDRO and DRO operation. If the plated wire is used in a DRO organization mode, the aging effect is only of secondary importance, because it does not limit memory operation. In the DRO mode, the tolerances on the environment and drive currents are more relaxed than in NDRO applications. Advantages of this technology are potential low costs and fast switching speeds.

The multilayer film technique offers a means of significantly reducing the number of interconnections in present magnetic thin-film arrays. It is estimated that array substrates fabricated by this technique have a potential packing density of 70,000 bits/in.^{3} By reducing the number of interconnections, reliability can be significantly improved.

The promising technologies detailed above for 1970-1972 are summarized in Table III.

TABLE III. – MOST LIKELY 1970-1972
MAIN MEMORY TECHNOLOGIES

DRO	NDRO
Magnetic Core	Plated Wire
Plated Wire	Bicore – Multilayer
Multilayer	Biax

For scratch-pad or high-speed control applications, bipolar integrated circuit memories show much promise. This type of memory technology is compatible with large-scale integration (LSI) techniques, and offers the advantages of high reliability high packing densities, and potential low cost.

In applications where an unalterable read-only memory is desired to guarantee integrity of information, the transformer-memory technique appears promising. This technique demonstrates proven reliability and is space-qualified from use in the Apollo guidance computer. The "braid," a variant of the transformer memory technique, is presently being developed to reduce the cost of fabrication. A loom is used as the means of manufacture of the transformer array.

SUMMARY AND CONCLUSIONS FOR AN ADVANCED GUIDANCE COMPUTER BREADBOARD

If it were desired at the present time to build a breadboard model of an advanced guidance computer, cost, availability, and delivery times are the constraining factors. On the assumption that such a breadboard were desired and that a 1-μsec R-W cycle time were required, a 3D coincident-current core memory system is a preferred technology for DRO applications. Magnetic-core memory systems are readily available and space-qualified, having proven their reliability in previous missions. The relatively fast R-W cycle time is required in order to implement advanced guidance systems.

Several NDRO memory technologies, the Biax, and Bicore or Quadralloy element, and multi-aperture devices, may be used in the breadboard for NDRO memory applications. Biax memories are presently available at modest costs. This memory technique is space-qualified from incorporation in avionics computers. Compared to the Bicore element, it has output signals about 10:1 greater, requires less read power, and has a better packing density. Also, the number of connections required per word is about one-third the number for the Bicore. This is because a transformer drive is usually used for the Bicore in view of the requirement of large drive currents. However, the Biax is a discrete element and is limited to a read-modify-write speed of about 5 μsec.

The Bicore or Quadralloy is a flight-qualified element, and is presently being used in aerospace computers. The Quadralloy element operates successfully in the Phoenix

guidance computer system, and is being designed into other computers. In a read-modify-write mode, present achievable cycle times are 7.5 μsec. Its main disadvantage is the requirement of relatively high drive currents – 1.5 A for write, 800 mA for read, and 100 mA for digit.

The multi-aperture device is available in the form of the transfluxor or the shmoo element. This type of memory exhibits large sense voltages (25 mV) enabling relatively easy detection of "1" and "0" information. Memories of this type are expensive, however, because of relatively intricate wiring. The devices also have severe temperature limitations.

Table IV shows in summary form the preferred technologies available for use in an advanced guidance computer breadboard.

TABLE IV. – PRESENT MAIN MEMORY TECHNOLOGIES

DRO	NDRO
Magnetic Core	Biax
----	Bicore
----	Multi-Aperture Devices

A fixed memory has limited usefulness in a breadboard because it may inhibit the flexibility of the breadboard computer as a laboratory tool and the guidance system of which it may be a part. It is anticipated that much software development may be done after fabrication of the breadboard computer, to determine the best executive routines for the computer, diagnostic routines, and algorithms for advanced guidance calculations. In order to do this, it is preferable that all main memory locations be electrically alterable.

CONCLUSIONS

A review of present guidance computer main memories is given, and anticipated developments for these main memory technologies by 1972 are detailed. Also, a discussion of NDRO- vs. DRO-type memories and of read-only memories is presented.

The technologies considered are magnetic cores, plated wire, planar-magnetic thin films, etched-permalloy toroids, monolithic ferrites, and integrated circuit memories. In Table I, the major characteristics of these technologies at the present time are identified. Table II lists an estimate of their characteristics by 1972. Table III presents promising technologies for use in a prototype version for 1970-1972, relative to a high-reliability and low-power space application. In addition, Table IV summarizes those technologies available for the implementation of an advanced guidance computer concept breadboard in 1967, if desired.

REFERENCES

1. Hobbs, L. C.: Present and Future State of the Art in Computer Memories. IEEE Transactions on Electronic Computers, Aug. 1966, pp. 534-549.

2. Gilligan, T.: 2-1/2D High Speed Memory Systems – Past, Present and Future. IEEE Transactions on Electronic Computers, Aug. 1966, pp. 475-485.

3. Rajchman, J.; and Lo, A. W.: The Transfluxor. Proceedings of the IRE, vol. 44, Mar. 1956, pp. 321-332.

4. Wanlass, C.; and Wanlass, S.: Biax High Speed Magnetic Computer Element. WESCON, 1959, pp. 40-54.

5. Danylchuk, I.; and Perreski, A. J.: Plated Wire Magnetic Film Memories. Proceedings 1964 INTERMAG Conference, pp. 5-4-1 to 5-4-6.

6. Maeda, H.; and Matsushita, A.: Woven Thin-Film Memories. Proceedings INTERMAG Conference, 1964, pp. 8-1-1 to 8-1-6.

7. Petschauer, R.; and Turnquist, R.: A Non-Destructive Readout Film Memory. Proceedings of the Western Joint Computer Conference, 19 May 1961.

8. Pohm, A.; Smay, T.; and Mayer, W.: A $.25 \times 10^6$ Bit, High Density Low Power NDRO Film Memory. Proceedings 1967 INTERMAG Conference.

9. Fuller, H. W.; McCormack, T. L.; and Brittard, C. R.: Batch Fabricated Matrix Memories. Proceedings Fall Joint Computer Conference, 1965, pp. 1035-1052.

10. Shahbender, R.; Wentworth, C.; Ki, K.; Hotchkiss, S.; and Rajchman, J. A.: Laminated Ferrite Memory. Proceedings Fall Joint Computer Conference, 1965, pp. 77-90.

11. Perkins, H. A.; and Schmidt, J. D.: Integrated Semiconductor Memory System. Proceedings Fall Joint Computer Conference, 1965, pp. 1053-1064.

12. Kittner, P.: The Rope Memory, A Permanent Storage Device. AFIP's Conf. Proc., vol. 24, pp. 45-58, Oct. 1963.

13. Aldrich, W.; and Alonso, R.: The "Braid" Transformer Memory. IEEE Transactions on Electronic Computers, Aug. 1966, pp. 502-508.

14. Lowell, A.; Mitsutomi, T.; Matsumoto, R.; and Burnett, G.: Silicon-On-Sapphire Batch Fabrication of Computer Logic and Memories. Aeronautical Electronics, National Conference Proceedings, 1966.

15. Manoni, L.: Modular Computer Design for Improved Reliability in Aerospace Vehicle Guidance and Control Systems. AGARD Guidance and Control Panel Symposium, May, 1967.

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS: Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

TECHNICAL NOTES: Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

TECHNICAL MEMORANDUMS: Information receiving limited distribution because of preliminary data, security classification, or other reasons.

CONTRACTOR REPORTS: Scientific and technical information generated under a NASA contract or grant and considered an important contribution to existing knowledge.

TECHNICAL TRANSLATIONS: Information published in a foreign language considered to merit NASA distribution in English.

SPECIAL PUBLICATIONS: Information derived from or of value to NASA activities. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

TECHNOLOGY UTILIZATION PUBLICATIONS: Information on technology used by NASA that may be of particular interest in commercial and other non-aerospace applications. Publications include Tech Briefs, Technology Utilization Reports and Notes, and Technology Surveys.

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION DIVISION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546